WHAT IS CLAIMED IS:

1. A method of forming an electrically conductive via, the method comprising the steps of:

forming a first electrically conductive layer,

forming a second layer on the first layer, the second layer having desired barrier layer properties,

forming a third non electrically conductive layer on the second layer,

etching a via hole through the third layer, the via hole having sidewalls and a bottom, thereby exposing a portion of the second layer at the bottom of the via hole,

redistributing the exposed portion of the second layer at the bottom of the via hole so that at least a portion of the second layer is removed from the bottom of the via hole and deposited on lower portions of the sidewalls of the via hole, and

forming a fourth electrically conductive layer within the via hole to form the electrically conductive via.

2. The method of claim 1, wherein the first layer is formed of copper.

3. The method of claim 1, wherein the second layer is a cobalt tungsten phosphorous alloy.

4. The method of claim 1, wherein the third layer is a low k material.

5. The method of claim 1, wherein the fourth layer is copper.

6. The method of claim 1, wherein the via and the via hole have aspect ratios that are at least two.

7. The method of claim 1, wherein the steps of etching the via hole and redistributing the exposed portion of the second layer are accomplished with the same process.

8. The method of claim 1, wherein the step of etching the via hole comprises a sputter etch.

9. The method of claim 1, wherein the step of etching the via hole comprises a wet etch.

10. The method of claim 1, wherein the step of etching the via hole comprises a reactive ion etch.

11. The method of claim 1, wherein the step of redistributing the exposed portion of the second layer comprises sputtering the second layer with a gas.

12. The method of claim 1, wherein the step of redistributing the exposed portion of the second layer comprises sputtering the second layer with argon.

13. The method of claim 1, wherein the step of redistributing the exposed portion of the second layer further comprises removing all of the second layer from the bottom of the via hole.

14. The method of claim 1, further comprising the step of forming a fifth layer of an electrically conductive material on the bottom and sidewalls of the via hole prior to the step of forming the fourth layer, where the fifth layer has desired barrier layer properties.

15. A via formed by the method of claim 1.

16. An integrated circuit, the improvement comprising a via formed by the method of claim 1.

17. An electrically conductive via for providing electrically continuity between a first electrically conductive layer and a second electrically conductive layer that are separated by a third non electrically conductive layer, the via including an electrically conductive plug, and a fourth barrier material at the bottom and lower sidewalls of the via.

18. The via of claim 17, further comprising a fifth barrier material on the bottom and sidewalls of the via.

19. An integrated circuit, the improvement comprising an electrically conductive via for providing electrically continuity between a first electrically conductive layer and a second electrically conductive layer that are separated by a third non electrically conductive layer, the via including an electrically conductive plug, and a fourth barrier material at the bottom and lower sidewalls of the via.

20. The integrated circuit of claim 19, further comprising a fifth barrier material on the bottom and sidewalls of the via.